Power Electronic Transformer with Reduced Number of Switches: Analysis of Input Clamp Circuit and a Modulation Strategy to Eliminate Input Snubber Requirement

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***Abstract*—This paper presents an analysis of the protective snubber circuits in a high frequency transformer (HFT) linked three phase ac/ac power conversion system with reduced number of switches. This topology provides single stage power conversion with bidirectional power flow capability and input power factor correction. This topology is important because of reduced number of switches in the voltage source side (usually the high voltage side). The presence of non-ideal leakage inductance in transformer windings necessitates the use of a snubber circuit for the safe commutation of leakage energy. A new modulation technique is proposed in order to reduce the protection requirements in the source side. This topology with the proposed control technique has been analyzed and simulated. The simulation results confirm the analysis and predicted advantages.**

I. Introduction

Matrix converter based three phase ac/ac power electronic systems have inherent bi-directional energy flow capability, power factor correction and single stage power conversion without any storage element. High frequency transformers (HFT) provide galvanic isolation along with voltage transformation. A major advantage being their small size compared to line frequency transformers. HFT linked matrix converter based three phase ac/ac systems, combine the advantages of both the matrix converter as well as the HFT. [1] provides an overview of the present day research in this area.

High Frequency Transformer (HFT) linked three-phase ac/ac systems are especially being explored in renewable energy applications because of their reduced size [2].

A HFT linked ac/ac system with reduced number of switches is proposed in [3]. This topology has only two control switches in the voltage source side, normally the high voltage one. From this point of view, this power electronic transformer system appears to be very promising in renewable energy applications. Due to the presence of non-ideal leakage inductances both in the primary and secondary windings of the transformers, any change in the switching state of the input or output side converter needs commutation of leakage energy. A clamp or a snubber circuit is used on both sides of the transformer for safe commutation of leakage currents. Commutation using a clamp circuit leads to power loss, output voltage loss, distortion in the output load current and common mode voltage switching [4]. Also, the clamp circuit involves an electrolytic capacitor (unreliable energy storing element) maintained at system level voltage. This also increases the voltage rating of the semiconductor switches present in the system.

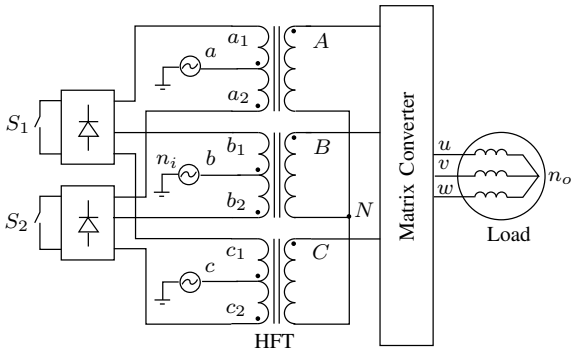

Fig. 1. High frequency transformer: push-pull topology

This paper, presents a comprehensive analysis of the input clamp circuit and the resulting limitations. A modulation strategy for the output side matrix converter has been proposed in order to obviate the need for an input clamp circuit.

II. Analysis of the input clamp circuit

In this topology, the input three phase balanced ac voltages are fed to a bank of three single phase transformers as shown in Fig. 1. S_1 and S_2 are switched in a complimentary fashion with 50% duty cycle. When switch S_1 is on, terminals a_1, b_1 and c_1 are shorted and the upper half of the primary windings conduct. Similarly, when S_2 is on, terminals a_2, b_2 and c_2 are shorted and power is transferred through the lower halves of the primary windings. The voltage across each secondary winding is a chopped version of the corresponding input line to neutral voltage. In the secondary side of the transformers, a matrix converter is employed in order to generate adjustable magnitude and frequency ac waveforms.

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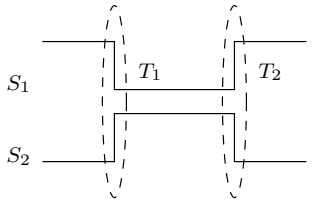

Fig. 2. Switching pulses for S_1 and S_2

During each switching transition of S_1 and S_2 (T_1 and T_2 as shown in Fig. 2), power flow is transferred from one half of the primary windings to the other. Due to the presence of leakage inductances L_1 and L_2 (Fig. 3) in the primary windings of the transformer, this transition is not instantaneous, and a snubber or clamp circuit is required for the commutation of the primary leakage energy. In Fig. 3, diodes d_{11}, d_{22} and the clamp capacitor C_l form the required clamp circuit. As both the transitions (T_1 and T_2) of S_1 and S_2 are symmetrical, here, a detailed analysis of T_1 is presented.

During T_1 and T_2, the output matrix converter is not switched. The secondary side matrix converter with three phase balanced load can be modeled as three phase balanced current sources ($i_A = I_A$, $i_B = I_B$ and $i_C = I_C$). Without any loss of generality, it is assumed that I_A is positive, while I_B and I_C are negative. Just before T_1, the currents i_{a_1}, i_{b_1} and i_{c_1} are equal to I_A, I_B and I_C respectively and i_{a_2}, i_{b_2} and i_{c_2} are all zero. The diodes, d_{a_1}, d_{b_2} and d_{c_2} are conducting to provide a path for these currents to flow through S_1. At T_1, when S_1 is switched off, the currents i_{a_1}, i_{b_1} and i_{c_1} cannot change instantaneously, this forces diode d_{11} to come into conduction and current starts flowing through the capacitor C_l.

In order to simplify the analysis, it is assumed that the two halves of the primary winding and the secondary winding have equal number of turns and L_1=L_2=L. Neglecting the magnetizing current, application of Amperes' law results in (1). In Fig. 3, two conducting loops can be traced involving upper halves of the primary windings. The KVL equations for these two loops are given by (2) and (3). By (1), if i_{a_1} reduces, the diode d'_{a_2} will turn on and the lower winding of phase a will start conducting. Similarly, for a desired change in currents i_{b_1} and i_{c_1}, diodes, d'_{b_1} and d'_{c_1} will start conducting. Switch S_2 provides a path for these currents to flow. The KVL equations for the two conducting loops with the lower halves of the primary windings are give by (4) and (5). In a balanced three phase system, with a floating neutral point, the three line to neutral values must sum to zero hence we obtain (6).

$$\begin{aligned} i_{a_1} - i_{a_2} - i_A &= 0 \\ i_{b_1} - i_{b_2} - i_B &= 0 \\ i_{c_1} - i_{c_2} - i_C &= 0 \end{aligned} \tag{1}$$

$$v_a - v_{a_1} - L\frac{d}{dt}i_{a_1} - V_{clp} + L\frac{d}{dt}i_{c_1} + v_{c_1} - v_c = 0 \tag{2}$$

$$v_a - v_{a_1} - L\frac{d}{dt}i_{a_1} - V_{clp} + L\frac{d}{dt}i_{b_1} + v_{b_1} - v_b = 0 \tag{3}$$

$$v_c + v_{c_1} - L\frac{d}{dt}i_{c_2} + L\frac{d}{dt}i_{a_2} - v_{a_1} - v_a = 0 \tag{4}$$

$$v_b + v_{b_1} - L\frac{d}{dt}i_{b_2} + L\frac{d}{dt}i_{a_2} - v_{a_1} - v_a = 0 \tag{5}$$

$$v_{a_1} + v_{b_1} + v_{c_1} = 0 \tag{6}$$

There are nine equations (1) to (6), involving six unknown rates of change of primary current and three unknown induced voltages in the transformer windings. The slope of the primary side currents are given by (7)- (9).

$$\frac{d}{dt}i_{a_1} = \frac{d}{dt}i_{a_2} = \frac{3v_a - V_{clp}}{3L} \tag{7}$$

$$\frac{d}{dt}i_{b_1} = \frac{d}{dt}i_{b_2} = \frac{6v_b + V_{clp}}{6L} \tag{8}$$

$$\frac{d}{dt}i_{c_1} = \frac{d}{dt}i_{c_2} = \frac{6v_c + V_{clp}}{6L} \tag{9}$$

When the switch S_1 is switched off and S_2 is switched on, the currents in the transformer are changing according to equations (7)-(9). When one of the three currents reaches zero, in the winding set connected to S_1 and the corresponding winding current connected to S_2 gets set to its desired value, the currents in the remaining phases, continue to flow at different rates. In the following analysis, let us assume that i_{b_1} goes to zero and i_{b_2} becomes I_B while, i_{a_1} and i_{c_1} are still positive and negative respectively. The network is changed because the branch containing diodes d_{b_1} and d_{b_2} has no current flowing through them and can be considered as an open circuit. All the equations remain the same as in the previous analysis except equation (3) is no longer valid, and the currents i_{b_1} and i_{b_2} do not change. In this stage, the slope of the currents, are given by (10)-(12).

$$\frac{d}{dt}i_{a_1} = \frac{d}{dt}i_{a_2} = \frac{2v_a - 2v_c - V_{clp}}{4L} \tag{10}$$

$$\frac{d}{dt}i_{b_1} = \frac{d}{dt}i_{b_2} = 0 \tag{11}$$

$$\frac{d}{dt}i_{c_1} = \frac{d}{dt}i_{c_2} = -\frac{2v_a - 2v_c - V_{clp}}{4L} \tag{12}$$

If the voltage across the clamp circuit capacitance (V_{clp}) is greater than 6 times the peak of the input line-neutral voltage (V_{ln_i}), all the primary currents during commutation will change in the desired direction. For example, in this case, i_{a_1} being positive, before T_1, should reduce to zero during commutation. Similarly, i_{a_2} should reduce to $-I_A$. This condition also ensures that once the primary currents reach their desired values, the commutation ends naturally. For example, once i_{a_1} reaches zero it remains there.

The primary snubber circuit is operational only two times during one switching period, the average current that flows through the clamp circuit per cycle is equal to the sum of the average value of i_{a_1} during T_1. For this case, the average clamp power loss is given by (13).

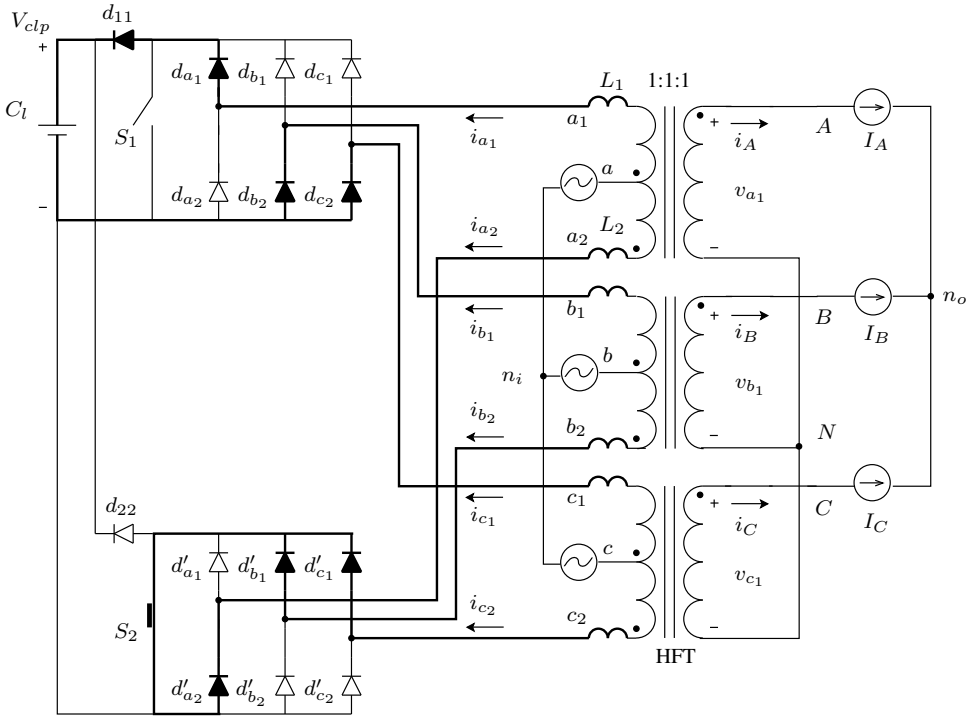

Fig. 3. Primary clamp circuit analysis

$$P_{pri} = \frac{1}{2} f_s L V_{clp} \left[\frac{3I_B^2}{6v_b + V_{clp}} - \frac{(I_A - I_C)^2}{2v_a - 2v_c - V_{clp}} \right] \quad (13)$$

From this analysis, the following points are evident 1) for the proper operation of the clamp circuit, V_{clp} has to be maintained greater than six times the line to neutral voltage. 2) From Fig. 3, when d_{11} conducts, the switch, S_1 has to block the voltage across the clamp circuit. 3) During the commutation, undesirable voltages are applied to the load, this leads to distortion in the output voltage and eventually in the output currents. 4) This commutation process also results in power loss given by (13).

A new modulation method is presented in the following section that overcomes these drawbacks.

III. A PWM TECHNIQUE TO ELIMINATE THE INPUT CLAMP CIRCUIT

The output side matrix converter transforms the high frequency output waveform of the transformer to an adjustable frequency and amplitude load voltage. When a zero vector is applied to the output load, the secondary currents i_A, i_B and i_C become zero. Then, S_1 and S_2 can be safely switched without the primary side snubber circuit.

Here, the modulation technique presented, applies a zero vector during T_1 and T_2. The input line to neutral voltages and the secondary side voltages are given by (14) and (15) respectively; where, $k = 0$ when S_1 is on and $k = 1$ when S_2 is on.

$$\begin{aligned} v_{an_i} &= V_i \cos(\omega_i t) \\ v_{bn_i} &= V_i \cos\left(\omega_i t - \frac{2\pi}{3}\right) \\ v_{cn_i} &= V_i \cos\left(\omega_i t + \frac{2\pi}{3}\right) \end{aligned} \quad (14)$$

$$\begin{aligned} v_{AN} &= (-1)^k v_{an_i} \\ v_{BN} &= (-1)^k v_{bn_i} \\ v_{CN} &= (-1)^k v_{cn_i} \end{aligned} \quad (15)$$

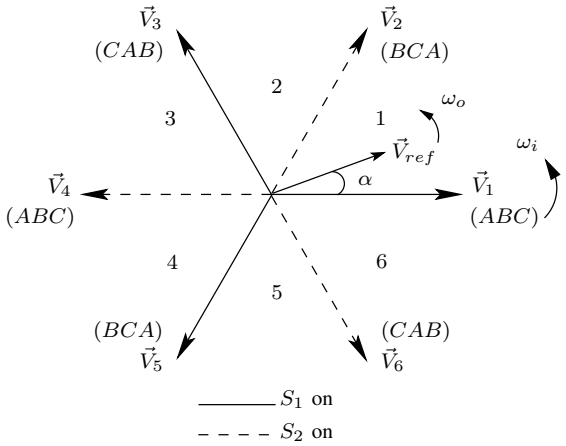

Fig. 4. CCW rotating vectors

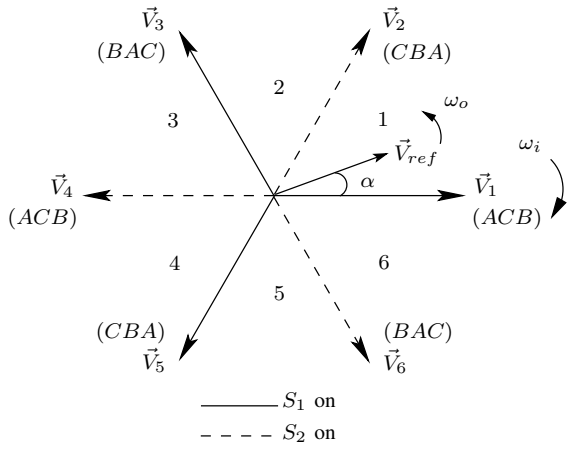

Fig. 5. CW rotating vectors

In a matrix converter, there are 27 unique switching states. Six of these switching states generate synchronously rotating space vectors [5]. These vectors result in zero common-mode voltage at the load terminals [6]. The output voltage space vector is defined by (16). Depending on the direction of rotation, these synchronously rotating vectors are further divided into two groups, counter-clockwise (ccw) and clockwise (cw). The three ccw rotating vectors $\vec{V}_1$, $\vec{V}_3$ and $\vec{V}_5$ marked in Fig. 4 are obtained when $k = 0$ and (uvw) are connected to (ABC), (CAB) and (BCA) respectively where, u, v, w, A, B, C are points marked in Fig. 1. For the same switching states, when $k = 1$, we obtain $\vec{V}_4$, $\vec{V}_6$ and $\vec{V}_2$ respectively. Similarly, the space vectors rotating in clockwise direction are shown in Fig. 5. Thus, every switching cycle, the average output voltage vector is synthesized using these six vectors (ccw or cw). These six vectors, divide the complex plane into six symmetrical sectors (marked in Fig. 4 and 5). At any instant of time, the reference voltage vector (defined by (17)) will be in a particular sector. This reference voltage vector is generated on an average over one T_s using the two vectors forming that sector. For example, if $\overline{V}_{ref}$ lies in the first sector, vectors $\vec{V}_1$ and $\vec{V}_2$ are used, such that $\overline{V}_{ref} = d_1\vec{V}_1 + d_2\vec{V}_2$, where d_1 and d_2 (given by (18)) are the fraction of time for which vectors $\vec{V}_1$ and $\vec{V}_2$ are applied respectively. The values of d_1 and d_2 are constrained to 0.5 because $\vec{V}_1$ and $\vec{V}_2$ are available for maximum 50% of the time. Hence, if only the two adjacent space vectors are used, the maximum modulation index, m is limited to 0.5. In [2], three adjacent voltage vectors are used to obtain a modulation index of 0.75 at the cost of additional switching.

$$\vec{V}_o = v_{un_o} + v_{vn_o}e^{j\frac{2\pi}{3}} + v_{wn_o}e^{-j\frac{2\pi}{3}} \tag{16}$$

$$\begin{aligned}
\overline{V}_{ref} &= \overline{V}_o = \overline{v}_{un_o} + \overline{v}_{vn_o}e^{j\frac{2\pi}{3}} + \overline{v}_{wn_o}e^{-j\frac{2\pi}{3}} \\
\overline{v}_{un_o} &= V_o\cos(\omega_o t + \phi) \\
\overline{v}_{vn_o} &= V_o\cos\left(\omega_o t + \phi - \frac{2\pi}{3}\right) \\
\overline{v}_{wn_o} &= V_o\cos\left(\omega_o t + \phi + \frac{2\pi}{3}\right)
\end{aligned} \tag{17}$$

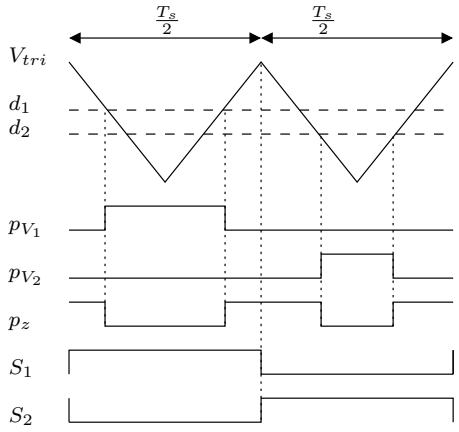

Fig. 6. Switching pulses for new modulation technique

TABLE I
SIMULATION PARAMETERS

V_i	100V
V_o	30V
ω_i	$2\pi60$ rad/sec
ω_o	$2\pi60$ rad/sec
Output power	1kW
Load pf.	0.8
L	12 μH
V_{clp}	600 V

The switching pulses for one cycle are shown in Fig. 6. The duty ratios d_1 and d_2 are compared with a triangular carrier waveform, V_{tri} to generate pulses p_{V_1} and p_{V_2}. V_{tri} has a peak value of 0.5 and its frequency is two times the frequency of S_1 and S_2. In sector one, $\vec{V}_1$ is available when S_1 is on, therefore, p_{V_1} is high in the first half of the cycle and p_{V_2} in the second half. Zero vectors are applied in the remaining time. p_z is the switching pulse for the zero vector. In each half cycle, the active vectors are buffered by zero vectors on either side. In one switching cycle, ccw vectors are used, and in the following cycle, cw vectors are used to synthesize the average output voltage. As ccw and cw rotating vectors are used for an equal duration of time, unity power factor is obtained on the input side [7].

$$\begin{aligned}
d_1 &= m\frac{2}{\sqrt{3}}\sin\left(\frac{\pi}{3} - \alpha\right) \\
d_2 &= m\frac{2}{\sqrt{3}}\sin(\alpha) \\
m &= \frac{V_o}{V_i}
\end{aligned} \tag{18}$$

IV. SIMULATION RESULTS

The curcuit in Fig. 3 is simulated in SABER. The leakage inductance value is chosen to be 12μH, and V_{clp} is kept at 700V. The instantaneous line to neutral voltages are set as follows $v_{an_i} = 100V$, $v_{bn_i} = -40V$ and $v_{cn_i} = -60V$. The

secondary side current sources I_A, I_B and I_C are set to 20A, -5A and -15A respectively. In Fig. 7 switch S_1 is turned off at 50μs (transition T_1). The currents i_{a_1}, i_{b_1} and i_{c_1} go to zero following the analytically predicted slopes. The current that flows into the clamp circuit is $i_{d_{11}}$, as expected it is the same as i_{a_1}.

A 1kW three phase AC-AC converter is simulated with the proposed modulation technique. The parameters used in the simulation are listed in Table I. Fig. 8(a) shows the input line to neutral voltage waveform with the corresponding filtered line current. This confirms input power factor correction. Fig. 8 (b) provides the sinusoidal output load current. The peak of this current is slightly lower than its analytically predicted value. This is due to the voltage loss resulting from the use of a secondary clamp circuit. From Fig. 9, it is observed that the currents through the primary side switches are zero when S_1 and S_2 are switched.

V. Conclusion

During the primary switching transitions, power is transferred from one primary winding to another. The commutation of leakage energy, requires a snubber circuit on the primary side. A detailed analysis of this circuit is presented and it is found that the input snubber circuit capacitance needs to be maintained at a very high voltage (greater than six times the line to neutral voltage). Note that usually, the primary is the high voltage side. This implies that the primary side switches have to be rated at very high value. Also, high rated blocking diodes, d_{11} and d_{22} are required on the primary side. A finite amount of time is required for the commutation of transformer leakage energy, hence, the values of d_1 and d_2 are lesser than 0.5.

A new modulation method is presented in this paper which has the following advantages,

1) Elimination of the primary clamp circuit which implies,
   - No power loss for input leakage inductance commutation.
   - No unreliable dc capacitor at a high voltage.
   - Reduction in the primary switch voltage rating.
2) Zero current switching (ZCS) for the input side converter.
3) Variable frequency and amplitude output voltage generation.

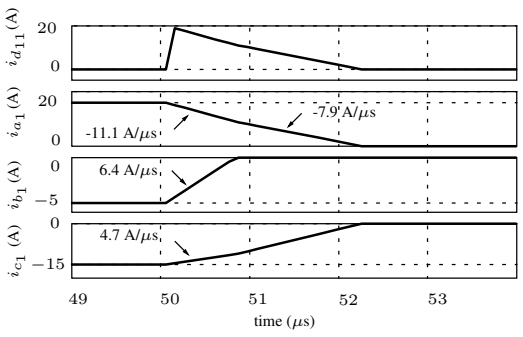

Fig. 7. Simulation result: input clamp circuit analysis

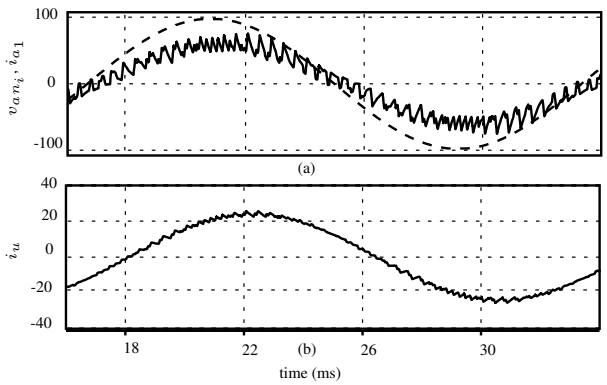

Fig. 8. Simulation result: Three phase ac-ac HFT using proposed modulation method (a) Input voltage (1V/div) and input current (0.1A/div) (b) Output current (1A/div)

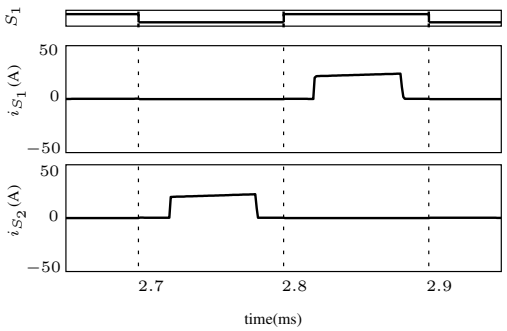

Fig. 9. Simulation result: Switching pulse and currents through switch S_1 and S_2

4) unity power factor correction.

The simulation results verify the advantages of the proposed modulation method. Although the proposed solution eliminates the primary clamp circuit, the secondary clamp circuit is still necessary. Due to the presence of leakage inductance on the primary side, loss less source based commutation (to remove the secondary clamp circuit) may not be possible in this topology. The secondary clamp circuit analysis needs to be done.

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